Sierra Components, Inc.

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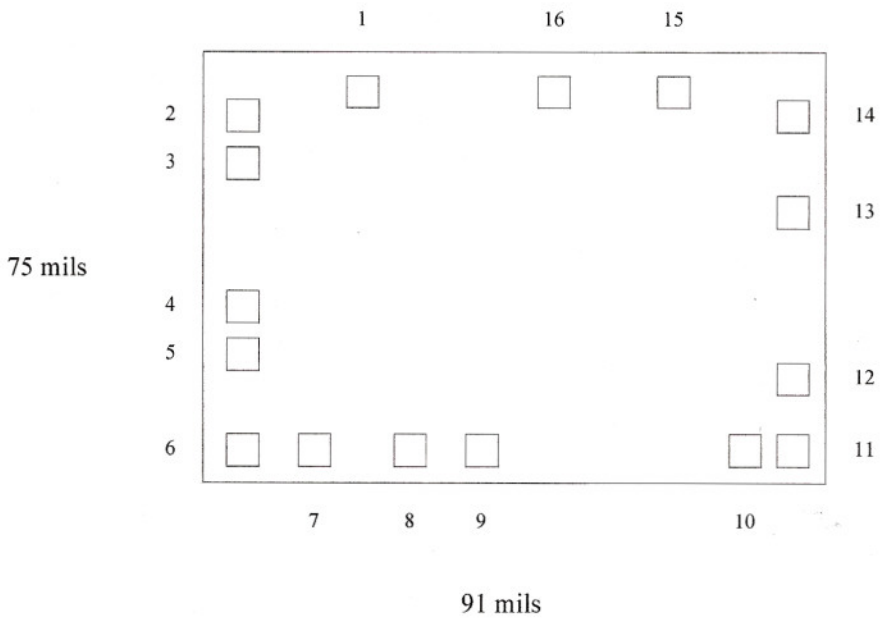
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



PAD	FUNCTION
1	Q3
2	P3
3	PE
4	INHIBIT
5	P0
6	CLOCK
7	Q0
8	V_{SS}
9	Q1
10	RESET
11	P1
12	"O"
13	CF
14	P2
15	Q2
16	V_{DD}

Topside Metal: Al
Backside: Si
Backside Potential: VDD
Mask Ref:
Bond Pads : .004"

APPROVED BY: CD	**DIE SIZE : .091"x .075"**	**DATE: 4/17/03**
MFG: Motorola	**THICKNESS: .015"**	**P/N: CD4526**

DG 10.1.2
Rev A 3-4-99